Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method of converting a first data path carrying P packets per system clock ~~processing~~ cycle to a second data path carrying Q packets per system clock ~~processing~~ cycle, wherein $Q < P$, comprising:

receiving the P packets during a first system clock ~~processing~~ cycle on the first data path;

storing the P packets in a queue;

shifting first data from the queue into a shift register;

selectively retrieving data from the shift register until a first set of Q packets of the P packets is retrieved, wherein the data from the shift register is selectively retrieved based on a determination of whether the data comprises one of an end-of-packet indicator, a data field, or a start-of-packet indicator; and

sending the set of Q packets on the second data path during the first system clock ~~processing~~ cycle, wherein the second path is coupled to a processing device configured to process a maximum of Q packets per system clock cycle.

2. (Currently amended) The method of claim 1, further comprising:

shifting second data from the queue into the shift register;

selectively retrieving data from the shift register until a second set of Q packets of the P packets is retrieved; and

sending the second set of Q packets on the second data path during a second system clock ~~processing~~ cycle.

3. (Original) The method of claim 1, wherein the queue comprises a first-in-first-out (FIFO) queue.

4-5. (Canceled)

6. (Currently amended) The method of claim 1 [[5]], wherein the processing device comprises a Cyclical Redundancy Checker (CRC).

7. (Currently amended) A packet processing system, comprising:

a first data path configured to receive P packets during a first system clock ~~processing~~ cycle;

a queue configured to store the P received packets;

a shift register;

a control unit configured to:

shift data of the P packets from the queue into the shift register,

selectively retrieve data from the shift register until a first set of Q packets is retrieved, wherein $Q < P$ and wherein the data from the shift register is selectively retrieved based on a determination of whether the data comprises one of an end-of-

packet indicator, a data field, or a start-of-packet indicator, and

send the first set of Q packets on a second data path during the first ~~system clock processing~~ cycle; and

a processing device configured to:

process a maximum of Q packets per system clock cycle received from the shift register via the second data path.

8. (Currently amended) A method of converting a first data path carrying P packets per system clock ~~processing~~ cycle to a second data path carrying Q packets per system clock ~~processing~~ cycle, wherein $Q < P$, comprising:

receiving the P packets during a first system clock ~~processing~~ cycle on the first data path;

storing the P packets in a queue;

selectively shifting one or more first bytes ~~first data~~ of the P packets from the queue into a shift register;

determining whether the one or more first bytes ~~data~~ in the shift register comprises at least one of an end-of-packet byte ~~indicator~~, a data byte ~~field~~, ~~and~~ or a start-of-packet byte ~~indicator~~; and

sending, based on the determination, a first set of Q packets, comprising at least a portion of the one or more first bytes, on a second data path during the first system clock ~~processing~~ cycle, wherein the second data path is coupled to a processing device configured

to process only *Q* packets per system clock cycle.

9. (Currently amended) The method of claim 8, further comprising:

shifting one or more second bytes ~~second data~~ of the *P* packets from the queue into the shift register;

determining whether the one or more second bytes ~~data~~ in the shift register comprises at least one of an end-of-packet byte ~~indicator~~, a data byte ~~field~~, ~~and~~ or a start-of-packet byte ~~indicator~~; and

sending, based on the determination, a second set of *Q* packets, comprising at least a portion of the one or more second bytes, on the second data path during a second system clock ~~processing~~ cycle.

10. (Original) The method of claim 8, wherein the queue comprises a first-in-first-out (FIFO) queue.

11. (Canceled)

12. (Currently amended) The method of claim 8 [[11]], wherein the processing device comprises a Cyclical Redundancy Checker (CRC).

13. (Currently amended) A packet processing system, comprising:

a first data path configured to receive *P* packets during a first system clock ~~processing~~ cycle;

a queue configured to store the *P* packets;

a shift register; and

a control unit configured to:

selectively shift one or more bytes ~~data~~ from the queue into the shift register,

determine whether the one or more bytes ~~data~~ in the shift register comprises at least one of an end-of-packet byte ~~indicator~~, a data byte ~~field~~, ~~and~~ or a start-of-packet byte ~~indicator~~, and

send, based on the determination, a first set of *Q* packets, comprising at least a portion of the one or more bytes, on a second data path during the first system clock ~~processing~~ cycle, wherein $Q < P$ and wherein the second data path is coupled to a processing device configured to process only *Q* packets per system clock cycle.

14. (Currently amended) A method of processing packets, comprising:

receiving a plurality of packets on a first data path;

converting the plurality of packets on the first data path to a first packet on a second data path;

processing the first packet on the second data path during a first system clock ~~processing~~ cycle, wherein a processing device that is configured to process only one packet

per processing cycle processes the first packet on the second data path during the first system clock cycle;

converting the plurality of packets on the first data path to a second packet on the second data path; and

processing the second packet on the second data path during a second system clock ~~processing~~ cycle.

15. (Currently amended) The method of claim 14, wherein converting the plurality of packets on the first data path to the [[a]] first packet on the second data path further comprises:

shifting a first quantity of data of the plurality of packets into a shift register;

selectively retrieving data from the shift register until the first packet is retrieved; and

sending the first packet on the first data path during the first system clock ~~processing~~ cycle.

16. (Currently amended) The method of claim 15, wherein converting the plurality of packets on the first data path to the [[a]] second packet on the second data path further comprises:

shifting a second quantity of data of the plurality of packets into a shift register;

selectively retrieving data from the shift register until the second packet is retrieved; and

sending the second packet on the second data path during the first system clock ~~processing~~ cycle.

17. (Original) The method of claim 15, wherein the data from the shift register is selectively retrieved based on a determination of whether the data comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator.

18. (Canceled)

19. (Currently amended) The method of claim 14 [[18]], wherein the processing device processes the second packet on the second data path during the second system clock ~~processing~~ cycle.

20. (Currently amended) The method of claim 14 [[18]], wherein the processing device comprises a Cyclical Redundancy Checker (CRC).

21. (Currently amended) A packet processing system, comprising:

a first data path configured to receive P packets;

a second data path configured to carry Q packets during a first system clock ~~processing~~ cycle, wherein $Q < P$;

a processing unit configured to:

convert the received *P* packets on the first data path to a first set of *Q* packets on the second data path during the first system clock ~~processing~~ cycle,

convert the received *P* packets on the first data path to a second set of *Q* packets on the second data path during a second system clock ~~processing~~ cycle; and

a first processing device configured to process only *Q* packets per system clock cycle and further configured to:

process the first set of *Q* packets on the second data path during the first system clock ~~processing~~ cycle, and

process the second set of *Q* packets on the second data path during the second system clock ~~processing~~ cycle.

22. (Currently amended) A method of processing a plurality of packets using a single packet per system clock cycle processing device, comprising:

receiving the plurality of packets during a first system clock ~~processing~~ cycle;

storing the plurality of packets in a queue;

selectively shifting one or more first bytes ~~a first quantity of data~~ of the plurality of packets from the queue into a shift register;

selectively retrieving the one or more first bytes ~~data~~ from the shift register until a first packet of the plurality of packets is retrieved, wherein the one or more bytes ~~data~~ from the shift register is selectively retrieved based on a determination of whether the one or more bytes ~~data~~ comprises at least one of an end-of-packet byte ~~indicator~~, a data byte ~~field~~,

or a start-of-packet byte ~~indicator~~; and

processing the retrieved first packet during the first system clock ~~processing~~ cycle, wherein a processing device that is configured to process only one packet per system clock cycle processes the first packet during the first system clock cycle.

23. (Currently amended) The method of claim 22, further comprising:

selectively retrieving one or more second bytes ~~data~~ from the shift register until a second packet of the plurality of packets is retrieved; and

processing the retrieved second packet during a second system clock ~~processing~~ cycle.

24. (Original) The method of claim 22, wherein the queue comprises a first-in-first-out (FIFO) queue.

25-26. (Canceled)

27. (Currently amended) The method of claim 23 [[26]], wherein the [[a]] processing device that is configured to process only one packet per system clock ~~processing~~ cycle processes the second packet during the second system clock ~~processing~~ cycle.

28. (Currently amended) The method of claim 22 [[26]], wherein the processing

device comprises a Cyclical Redundancy Checker (CRC).

29. (Currently amended) A packet processing system, comprising:

a first data path configured to receive a plurality of packets during a first system clock ~~processing~~ cycle;

a queue configured to store the plurality of packets;

a control unit configured to:

selectively shift one or more bytes ~~a first quantity of data~~ of the plurality of packets from the queue into a shift register, and

selectively retrieve the one or more bytes ~~data~~ from the shift register until a first packet of the plurality of packets is retrieved, wherein the one or more bytes ~~data~~ from the shift register is selectively retrieved based on a determination of whether the one or more bytes ~~data~~ comprises one of an end-of-packet byte ~~indicator~~, a data byte ~~field~~, or a start-of-packet byte ~~indicator~~; and

a packet processing device configured to process only one packet per system clock cycle and further configured to process the retrieved first packet during the first system clock ~~processing~~ cycle.

30-33. (Canceled)